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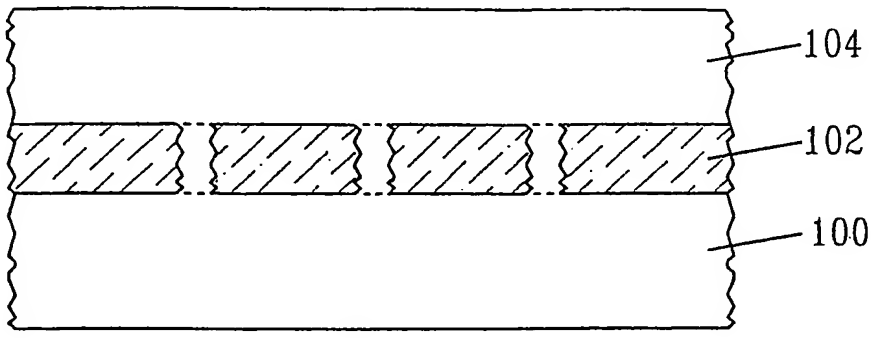
(54) Title: THIN BURIED OXIDES BY LOW-DOSE OXYGEN IMPLANTATION INTO MODIFIED SILICON



(57) Abstract: A method of fabricating silicon-on-insulators (SOIs) having a thin, but uniform buried oxide region beneath a Si-containing over-layer is provided. The SOI structures are fabricated by first modifying a surface of a Si-containing substrate to contain a large concentration of vacancies or voids. Next, a Si-containing layer is typically, but not always, formed atop the substrate and then oxygen ions are implanted into the structure utilizing a low-oxygen dose. The structure is then annealed to convert the implanted oxygen ions into a thin, but uniform thermal buried oxide region.

WO 2005/034209 A2

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THIN BURIED OXIDES BY LOW-DOSE OXYGEN IMPLANTATION INTO MODIFIED SILICON

DESCRIPTION

Field of the Invention

[0001] The present invention relates to a method of fabricating a semiconductor structure, and more particularly to a method of fabricating a silicon-on-insulator (SOI) having a thin, uniform buried oxide, less than 100 nm in thickness, that is formed by using low-dose oxygen implantation.

Background of the Invention

[0002] Silicon-on-insulator (SOI) structures are used in microelectronic device applications where the electrical and electronic interactions between the active device region and the underlying semiconductor structure are strongly discouraged. In a typical SOI structure, the buried oxide layer separates the Si over-layer (i.e., the SOI or device layer) from the Si substrate.

[0003] In complementary metal oxide semiconductor (CMOS) devices built on SOI, for instance, performance characteristics are known to be greatly improved. Specifically CMOS devices built on SOI can exhibit less junction capacitance and leakage, greater resistance to ionizing radiation, immunity to latch-up, etc. However, forming SOI structures is no simple matter.

[0004] Even after decades of research and development only a few methods are proven to be commercially viable. In one, called BESOI (bond-and-etch-back SOI), two Si wafers are oxidized at the surface and the oxidized surfaces are bonded together and then one of the two bonded wafers is etched to provide a thin SOI device layer. In this prior art method and its variations, as the wafer surfaces are oxidized before bonding, the

buried oxide can be made to have any desired thickness. However, impurities at the bonded interface and the difficulty in achieving a thin, uniform Si over-layer through the etch-back process are major drawbacks. The terms "Si over-layer" and "SOI layer" may be interchangeably used in this application.

[0005] In another well-known method, called SIMOX (separation by implantation of oxygen), a selected dose of oxygen ions is directly implanted into a Si wafer, and then the wafer is annealed in an oxygen ambient at a high temperature so that the implanted oxygen is converted into a continuous buried oxide layer. The thickness of the buried oxide layer in the SIMOX method is mostly dependent on the implanted oxygen dose and the thermal oxidation conditions. Moreover, in SIMOX, the Si over-layer is thinned to a desired thickness during the thermal oxidation, after which the surface oxide is stripped off.

[0006] When the peak concentration of the implanted oxygen is very low (on the order of about 1E22 atoms/cm^3 or less), however, the buried oxide typically becomes broken and discontinuous, as the growing oxide precipitates tend to ball up to minimize the surface energy. Such an SOI structure is shown, for example, in FIG. 1. In FIG. 1, reference numeral 100 denotes the Si-containing substrate layer, reference numeral 102 denotes the buried oxide and reference numeral 104 denotes the Si-containing over-layer of a prior art SOI structure. As such, it is generally very difficult to form a buried oxide layer thinner than 100 nm using conventional SIMOX processing.

[0007] In MOSFET device applications, the Si over-layer and the buried oxide underneath need to be made thinner as the device dimensions shrink, in order to better control short-channel effects. This means that the buried oxide in up coming generations of MOSFET devices needs to be far thinner than what the conventional SIMOX technology is capable of.

Summary of the Invention

[0008] One object of the present invention is to provide a method of fabricating SOI structures with a very thin (less than 100 nm), but uniform buried oxide.

[0009] Another object of the present invention is to provide a method of fabricating SOI structures in which the processing time is reduced, yet the throughput is increased by reducing the oxygen implantation dose to a level below which is allowed for in a typical SIMOX process.

[0010] An even further object of the present invention is to provide a method of fabricating SOI structures where the defect level in the Si over-layer, i.e., the SOI layer, is reduced by reducing implantation damages and by reducing the stresses and strains from the expanding volume of the buried oxide.

[0011] These and other objects and advantages are achieved in the present invention by utilizing a method wherein a low-dose oxygen implantation step is performed. By "low-dose", it is meant an oxygen dose of about 1E17 atoms/cm^2 or less. In prior art SIMOX processes, a low-dose oxygen implantation would usually result in a layer of broken and discontinuous buried oxides as the oxide tends to ball up to minimize surface energy. In the present invention, the problem is solved by forming a large number of vacancies or voids in a Si-containing substrate prior to the low-dose oxygen implantation step.

[0012] The vacancies or voids coalesce during the subsequent high-temperature oxidation and provide room for the buried oxide to expand laterally, resulting in a thin, uniform buried oxide layer. The term "uniform" is used in the present invention to denote a buried oxide region having a continuous interface with the Si-containing over-layer as well as the underlying Si-containing substrate wherein the variation of thickness across the entire wafer is less than 30 % of the total thickness of the buried oxide layer. With a sufficient density of vacancies or voids, the thickness of the buried oxide layer is

mostly dependent on the implanted dose and the internal thermal oxidation conditions. In one embodiment of the present invention, the vacancies or voids are formed into a Si-containing substrate by utilizing an electrolytic anodization process wherein a HF-containing solution is used.

[0013] In accordance with the method of the present invention, the SOI structure is fabricated by modifying a surface of a Si-containing substrate to contain a large concentration (on the order of about 0.01 % or greater) of vacancies or voids. The terms "vacancies" and "voids" are interchangeably used in the present invention to denote a porous Si region. Next, a Si-containing layer is typically, but not always, formed atop the substrate and then oxygen ions are implanted into the structure utilizing a low-oxygen dose. The structure is then annealed to convert the implanted oxygen ions into a thin, but uniform thermal buried oxide region.

[0014] In broad terms, the method of the present invention comprises the steps of:

[0015] providing a structure comprising at least a Si-containing substrate that has a region of vacancies or voids located therein;

[0016] optionally forming a single crystal Si-containing layer atop said structure;

[0017] implanting oxygen ions into said structure using an oxygen dose of about 1E17 atoms/cm^2 or less; and

[0018] annealing the structure containing implanted oxygen ions and vacancies or voids to form a silicon-on-insulator that includes a Si-containing over-layer and a buried oxide, said buried oxide having a thickness of about 100 nm or less.

[0019] In some embodiments of the present invention, a bake step conducted in a hydrogen-containing ambient is employed prior to the optional forming a single crystal Si-containing layer over the porous structure or prior to the implanting step.

[0020] In yet another embodiment of the present invention, a baking step performed in a hydrogen-containing atmosphere is employed to the SOI structure which includes the thin buried oxide layer.

[0021] The SOI structure obtained from the present invention contains a very thin, yet uniform and continuous buried oxide region.

Brief Description of the Drawings

[0022] FIG. 1 is a pictorial representation (through a cross sectional view) of a prior art SOI structure made from a conventional SIMOX process using a low-dose oxygen implantation step.

[0023] FIGS. 2A-2H are pictorial representations (through cross sectional views) illustrating the basic processing steps of the present invention.

[0024] FIGS 3A-3C are cross-sectional SEM images through various processing steps of the present invention.

Detailed Description of the Invention

[0025] The present invention, which provides a simple and low-cost method for forming an SOI substrate having a thin, uniform buried oxide region underlying a Si-containing overlayer, will now be described in greater detail by referring to the drawings that accompany the present application. In the accompanying drawings, like and/or corresponding elements are referred to by like reference numerals.

[0026] Reference is first made to the initial structure shown in FIG. 2A, which includes a Si-containing substrate 10 having a region 12 of vacancies or voids formed therein. The terms "vacancies" and "voids" are interchangeable used in the present invention to denote a porous Si-containing region. The term "Si-containing" as used herein denotes a semiconductor material that includes at least silicon. Illustrative examples of such Si-containing materials include, but are not limited to: Si, SiGe, SiC, SiGeC, epi-Si/Si, epi-Si/SiC, epi-Si/SiGe, and preformed silicon-on-insulators (SOIs) or SiGe-on-insulators (SGOIs) which may include any number of buried insulating (i.e., continuous, non-continuous or a combination of continuous and non-continuous) regions formed therein.

[0027] The Si-containing substrate is a doped substrate that may contain a p- or n-type dopant, with p-type dopants being highly preferred. Doping is achieved either by growing doped Si ingots from which p- or n-doped wafers are cut and polished, or by ion implantation. Both of the aforementioned doping processes are well known to those skilled in the art. The concentration of dopants within the initial Si-containing substrate 10 may vary depending on the dopant used. For n-type dopants, the concentration of dopant being implanted is typically from about 1E17 to about 1E18 atoms/cm^3, whereas for p-type dopants, the concentration of dopant being implanted is typically from about 1E15 to about 2E19 atoms/cm^3.

[0028] Region 12 is formed near a surface region of the Si-containing substrate 10 using an electrolytic anodization process that is capable of forming a porous Si-containing region in the Si-containing substrate 10. The porous Si-containing region, i.e., region 12, includes vacancies or voids therein. The anodization process is performed by immersing the structure shown in FIG. 2A into an HF-containing solution while an electrical bias is applied to the structure with respect to an electrode also placed in the HF-containing solution. In such a process, the p-type structure typically serves as the positive electrode of the electrochemical cell, while another semiconducting material such as Si, or a metal is employed as the negative electrode.

[0029] In general, the HF anodization converts doped single crystal Si into porous Si. The rate of formation and the nature of the porous Si so-formed (porosity and microstructure) is determined by both the material properties, i.e., doping type and concentration, as well as the reaction conditions of the anodization process itself (current density, bias, illumination and additives in the HF-containing solution). Specifically, the porous Si forms with greatly increased efficiency in the higher doped regions.

[0030] Generally, the porous Si-containing region 12 formed in the present invention has a porosity of about 0.01% or higher. The depth of the porous Si-containing region 12 is typically from about 1000 nm or less, as measured from the upper most surface layer of the Si-containing substrate 10.

[0031] The term "HF-containing solution" includes concentrated HF (49%), concentrated HF with acetic acid, a mixture of HF and water, a mixture of HF and a monohydric alcohol such as methanol, ethanol, propanol, etc, or HF mixed with at least one surfactant. The amount of surfactant that is present in the HF solution is typically from about 1 to about 50%, based on 49% HF.

[0032] The anodization process, which converts a near surface portion of the Si-containing substrate 10 into a porous Si-containing region 12 using a constant current source that operates at a current density of from about 0.05 to about 50 milliAmps/cm^2. A light source may be optionally used to illuminate the sample. More preferably, the anodization process of the present invention is employed using a constant current source operating at a current density of from about 0.1 to about 5 milliAmps/cm^2.

[0033] The anodization process is typically performed at room temperature or at a temperature that is elevated from room temperature may be used. Following the anodization process, the structure is typically rinsed with deionized water and dried.

[0034] In an optional embodiment of the present invention, the structure shown in FIG. 2A may be baked in a hydrogen-containing ambient at atmospheric or a reduced pressure at this point of the present invention. When performed, this optional embodiment desorbs impurity atoms from the porous Si-containing region 12 (i.e., region containing vacancies and voids), while at the same time closing up any surface pores. The bake in a hydrogen-containing ambient is performed at a temperature from about 800° to about 1200°C, with a temperature from about 1000° to about 1150°C being more highly preferred. Examples of hydrogen-containing ambients include H_2, NH_4, or mixtures thereof, including mixtures with, or without, an inert gas.

[0035] Next, a single crystal Si-containing layer 14 is typically, but not always, formed atop the Si-containing substrate 10 containing the porous Si-containing region 12 at this point of the present invention. The single crystal Si-containing layer 14 may not be needed when the porous Si-containing region 12 is formed some distance, 50 nm or greater, below the surface of the Si-containing substrate 10. The structure including the single crystal Si-containing layer 14 is shown, for example, in FIG. 2B; reference numeral 13 denotes the interface between the porous Si-containing region 12 and the single crystal Si-containing layer 14. The single crystal Si-containing layer 14 employed in the present invention comprises any Si-containing material including, for example, epitaxial Si (epi-Si), amorphous Si (a:Si), SiGe, single or polycrystalline Si or any combination thereof. Of the various Si materials listed above, it is preferred that epi-Si or epi-SiGe be employed as the single crystal Si-containing layer 14.

[0036] The single crystal Si-containing layer 14 has a thickness of from about 1 to about 1000 nm, with a thickness of from about 1 to about 400 nm being more highly preferred. The single crystal Si-containing layer 14 is formed using known deposition processes including an epitaxial growth process.

[0037] The structure including the thus formed porous Si-containing region 12, with the single crystal Si-containing layer 14 is then implanted with oxygen ions. The

implant step may be a blanket implant in which oxygen ions are implanted across the entire wafer. This embodiment is depicted in FIG. 2C wherein region 16 denotes the oxygen implant region. The oxygen implant step may vary such that the oxygen peak is located at the Si-containing layer/porous Si interface or within the porous Si region (not shown). FIG. 2D depicts an embodiment in which a patterned oxygen ion implant step is performed forming patterned regions of implanted oxygen ions. Reference numeral 16' denotes the patterned regions of implanted oxygen ions.

[0038] The oxygen implant step is preformed using a low-dose implantation process. By "low-dose" it is meant an implant process in which the dose of oxygen ions being implanted into the Si-containing structures is about 1E17 atoms/cm^2 or less at greater than 200°C. More preferably, the oxygen implant step of the present invention is performed using a dose of oxygen ions from about 1E16 to about 5E16 atoms/cm^2. The implant may be performed in a continuous mode, or the implant may be performed using a pulse mode.

[0039] The low-dose oxygen ion implant step of the present invention is performed using a conventional implanter in which a beam current density from about 0.05 to about 500 milliAmps/cm^2, with a beam current density from about 5 to about 50 milliAmps/cm^2 being more typical, is employed. The low-dose oxygen implant step of the present invention is typically performed at a temperature from about 200° to about 600°C. More typically, the temperature in which the implant is performed is from about 200° to about 400°C. The implant is performed at an energy from about 40 to about 1000 keV, with an energy from about 100 to about 200 keV being more typical.

[0040] In addition to the foregoing base oxygen implant step, an optional second oxygen implant step may be performed to enhance the uniformity of the buried oxide to be subsequently formed. The optional second oxygen implant step is performed at a dose of about 1E17 atoms/cm^2 or less. More preferably, the optional second oxygen implant step is performed using a dose of oxygen ions from about 1E14 to about 1E16

atoms/cm^2. The implant may be performed in a continuous mode, or the implant may be performed using a pulse mode.

[0041] The optional second oxygen ion implant step of the present invention is performed using a beam current density from about 0.05 to about 5 milliAmps/cm^2. The optional second oxygen implant step of the present invention is typically performed at a temperature from about 4K to about 200 °C. More typically, the temperature in which the optional implant is performed is from about nominal room temperature to about 100°C. The optional implant step is performed at an energy from about 40 to about 1000 keV, with an energy from about 100 to about 200 keV being more typical.

[0042] The low-dose oxygen implant step forms an oxygen implant region 16 that has a depth, as measured from the upper surface of the Si-containing substrate 10 of about 1500 nm or less. More preferably, the depth of the oxygen implant region 16 is from about 100 to about 500 nm. The depth of the oxygen implant region 16 should preferably be at the center or slightly below interface 13.

[0043] Subsequently, the structure shown in FIGS. 2C or 2D is heated, i.e., annealed, using an oxidation process at a temperature at which the implant oxygen precipitates as oxides, and the precipitated oxides combine to form a thin, uniform buried oxide layer 18. A lot of the pores in the porous Si-containing region 12 are consumed during the thermal oxidation process and the remaining ones, if any, typically collapse into several large voids. In some embodiments in which the initial Si-containing substrate contains boron as a p-type dopant, the boron diffuses out from the starting substrate during this thermal oxidation step. The resultant structure including buried oxide region 18 and Si-containing over-layer 20, i.e., the SOI layer, is shown, for example, in FIG. 2E and 2F.

[0044] Note that an oxide layer 22 is formed atop the Si-containing over-layer 20 during the heating step. This surface oxide layer, i.e., oxide layer 22, is typically, but not always, removed from the structure after the heating step using a conventional wet etch

process wherein a chemical etchant such as HF that has a high selectivity for removing oxide as compared to silicon is employed. FIG. 2G or 2H shows the structure after the surface oxide layer 22 has been removed.

[0045] The thickness of the buried oxide and the Si-containing over-layer can be controlled to desired values by adjusting the thermal oxidation conditions. The surface oxide layer 22 formed after the heating step of the present invention has a variable thickness which may range from about 10 to about 1000 nm, with a thickness of from about 20 to about 500 nm being more typical.

[0046] Specifically, the heating step of the present invention is a thermal oxidation process that is performed at a temperature from about 650° to about 1350°C, with a temperature from about 1200° to about 1325°C being more highly preferred. Moreover, the heating step of the present invention is carried out in an oxidizing ambient which includes at least one oxygen-containing gas such as O_2, NO, N_2O, ozone, air and other like oxygen-containing gases. The oxygen-containing gas may be admixed with each other (such as an admixture of O_2 and NO), or the gas may be diluted with an inert gas such as He, Ar, N_2, Xe, Kr, or Ne. When a diluted ambient is employed, the diluted ambient contains from about 0.5 to about 100% of oxygen-containing gas, the remainder, up to 100%, being inert gas.

[0047] The heating step may be carried out for a variable period of time that typically ranges from about 10 to about 1800 minutes (at 1200° to about 1325°C), with a time period from about 60 to about 600 minutes being more highly preferred. The heating step may be carried out at a single targeted temperature, or various ramp and soak cycles using various ramp rates and soak times can be employed.

[0048] In another embodiment of the present invention wherein excess dopant ions are implanted, a post oxidation thermal anneal in a hydrogen ambient can be used to reduce the level of dopants within the Si-containing over-layer. When such a post

oxidation process is performed, the post oxidation thermal anneal in a hydrogen ambient is performed at a temperature from about 800° to about 1200°C, with a temperature from about 1000° to about 1150°C being more highly preferred. Examples of hydrogen ambients include H_2, NH_4, and mixtures thereof, including mixtures with, or without, an inert gas. The concentration of dopant ions with the Si-containing over-layer may be reduced by more than two orders of magnitude using the aforementioned post oxidation thermal anneal.

[0049] In yet another embodiment of the present invention, the single crystal Si-containing layer is not formed atop the Si-containing substrate containing the porous Si region. In this embodiment, the oxygen ions are directly implanted into the porous Si-containing substrate. This substrate may, or may not have undergone a H_2 bake treatment. The resulting buried oxide would be still uniform, but somewhat thicker due to faster oxygen diffusion from the ambient to the buried oxide during thermal oxidation.

[0050] In accordance with the present invention, the Si-containing over-layer 20 has a thickness of about 1000 nm or less, with a thickness of from about 10 to about 800 nm being more highly preferred. Note that the Si-containing over-layer 20 formed in the present invention is a thin layer that is substantially defect free. The buried oxide layer 18 formed during the heating step has a thickness of about 5 nm to about 100 nm, with a thickness of from about 10 to about 80 nm being more highly preferred. The buried oxide layer 18 has a smooth and continuous interface with the Si-containing over-layer 20.

[0051] As stated above, the surface oxide layer 22 may be stripped at this point of the present invention so as to provide the Si-on-insulator substrate material shown, for example, in FIG. 2G or 2H.

[0052] FIG. 3A is a cross-sectional SEM micrograph showing a buried oxide layer of approximately 12 nm thickness formed by the inventive method described here. The substrate process history was as follows:

- Starting substrate: Boron-doped wafers with p-doping of 1E19 cm^{-3}
- Porous-Si Formation: current, 0.5 – 1.0 mA, time: approximately 2 min
- Epi-Si growth: 4000–5000Å with a H_2 bake at 1150°C
- Oxygen implant @ 350°C: 5E16 cm^{-2}
- Oxygen implant @ nominal room temperature: 2E15 cm^{-2}
- High temperature anneal: 10 hrs @ 1325°C with approximately 25% oxygen mixed with Ar + 5 hrs @ 1325°C with approximately 35% oxygen mixed with Ar

Region A is the surface oxide grown during the anneal
Region B is the SOI layer
Region C is the thin buried oxide
Region D is the substrate

[0053] FIG. 3B is a cross-sectional SEM micrograph showing a broken buried oxide layer of approximately 76 nm islands. This region of the same substrate as above did not receive any porous-Si treatment but did receive the same Si epi growth, oxygen implants and anneals as shown in FIG. 3A. This figure clearly demonstrates that the existence of a porous-Si is the center piece to create a thin and continuous buried oxide. The substrate history is described below.

- Starting substrate: Boron-doped wafers with p-doping of 1E19 cm^{-3}
- Epi-Si growth: 4000–5000 Å with a H_2 bake at 1150°C
- Oxygen implant @ 350°C: 5E16 cm^{-2}
- Oxygen implant @ nominal room temperature: 2E15 cm^{-2}
- High temperature anneal: 10 hrs @ 1325°C with approximately 25% oxygen mixed with Ar + 5 hrs @ 1325°C with approximately 35% oxygen mixed with Ar

Region A is the surface oxide grown during the anneal
Region B is the SOI layer
Region C is that with broken buried oxide
Region D is the substrate

[0054] FIG. 3C is a cross-sectional SEM micrograph showing how the buried oxide layer thickness can be controlled by the base oxygen implant dose. Buried oxide of approximately 36 nm was created by the inventive method described here. The substrate process history was as follows:

- Starting substrate: Boron-doped wafers with p-doping of 1E19 cm^{-3}
- Porous-Si Formation: current, 0.5 – 1.0 mA, time: approximately 2 min
- Epi-Si growth: 4000-5000Å with a H_2 bake at 1150°C
- Oxygen implant @ 350°C: 1E17 cm^{-2}
- Oxygen implant @ nominal room temperature: 2E15 cm^{-2}
- High temperature anneal: 10 hrs @ 1325°C with approximately 25% oxygen mixed with Ar + 5 hrs @ 1325°C with approximately 35% oxygen mixed with Ar

Region A is the surface oxide grown during the anneal
Region B is the SOI layer
Region C is the thin buried oxide
Region D is the substrate

[0055] While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the scope and spirit of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method of fabricating a silicon-on-insulator (SOI) substrate comprising:

providing a structure comprising at least a Si-containing substrate that has a region of vacancies or voids located therein;

implanting oxygen ions into said structure using an oxygen dose of about 1E17 atoms/cm^2 or less; and

annealing the structure containing implanted oxygen ions and vacancies or voids to form a silicon-on-insulator that includes a Si-containing over-layer and a buried oxide, said buried oxide having a thickness of about 100 nm or less.

2. The method of Claim 1 wherein said Si-containing substrate is a doped substrate containing n- or p-type dopants.

3. The method of Claim 2 wherein said Si-containing substrate is a p-type substrate.

4. The method of Claim 1 wherein said providing step comprises an electrolytic anodization process.

5. The method of Claim 4 wherein said electrolytic anodization process is performed in the presence of a HF-containing solution.

6. The method of Claim 4 wherein the anodization process is performed using a constant current source operating at a current density of from about 0.05 to about 50 milliAmps/cm^2.

7. The method of Claim 1 wherein said region of vacancies or voids is a porous Si-containing region that has a porosity of about 0.01% or greater.

8. The method of Claim 1 further comprising forming a single crystal Si-containing layer between said providing and said implanting steps.

9. The method of Claim 8 wherein said single crystal Si-containing layer comprises epitaxial Si, amorphous Si, SiGe, single or polycrystalline Si or any combinations thereof.

10. The method of Claim 1 further comprising a bake step between said providing and said implanting steps, with or without subsequent Si-containing layer growth.

11. The method of Claim 10 wherein said bake step is performed in a hydrogen-containing ambient at a temperature from about 800° to about 1200°C.

12. The method of Claim 1 wherein said implanting step is performed at an ion dose from about 1E16 to about 1E17 atoms/cm^2.

13. The method of Claim 1 wherein said implanting step is performed using a beam current density from about 0.05 to about 500 milliAmps/cm^2, an energy from about 40 to about 100O keV, and a temperature from about 200° to about 600° C.

14. The method of Claim 1 wherein said implanting step is a blanket implant process.

15. The method of Claim 1 wherein said implanting step is a patterned implant process.

16. The method of Claim 1 wherein said implanting step further comprises a second oxygen implant step.

17. The method of Claim 16 wherein said second implant step is performed at an oxygen dose from about 1E14 to about 1E16 atoms/cm^2 using a beam current density from about 0.05 to about 5 milliAmps/cm^2, an energy from about 40 to about 1000 keV, and a temperature from about 4K to about 200° C.

18. The method of Claim 1 wherein the annealing is performed in an oxygen-containing ambient.

19. The method of Claim 18 wherein the oxygen-containing ambient further comprises an inert gas.

20. The method of Claim 19 wherein the oxygen-containing ambient is selected from the group consisting of O_2, NO, N_2O, ozone, and air.

21. The method of Claim 1 wherein the annealing is performed at a temperature of from about 650°C to about 1350°C.

22. The method of Claim 1 wherein the annealing forms a surface oxide atop the Si-containing over-layer.

23. A method of fabricating a silicon-on-insulator (SOI) substrate comprising:

providing a structure comprising at least a Si-containing substrate that has a region of vacancies or voids located therein;

forming a single crystal Si-containing layer atop said structure;

implanting oxygen ions into said structure using an oxygen dose of about 1E17 atoms/cm^2 or less; and

annealing the structure containing implanted oxygen ions and vacancies or voids to form a silicon-on-insulator that includes a Si-containing over-layer and a buried oxide, said buried oxide having a thickness of about 100 nm or less.

24. A method of fabricating a silicon-on-insulator (SOI) substrate comprising:

providing a structure comprising at least a Si-containing substrate that has a region of vacancies or voids located therein;

subjecting said structure to a bake step, said bake step is performed in a hydrogen-containing ambient;

implanting oxygen ions into said structure using an oxygen dose of about 1E17 atoms/cm^2 or less; and

annealing the structure containing implanted oxygen ions and vacancies or voids to form a silicon-on-insulator that includes a Si-containing over-layer and a buried oxide, said buried oxide having a thickness of about 100 nm or less.

25. The method of Claim 24 further comprising forming a single crystal Si-containing layer atop said structure, said forming step occurs between said subjecting and said implanting steps.

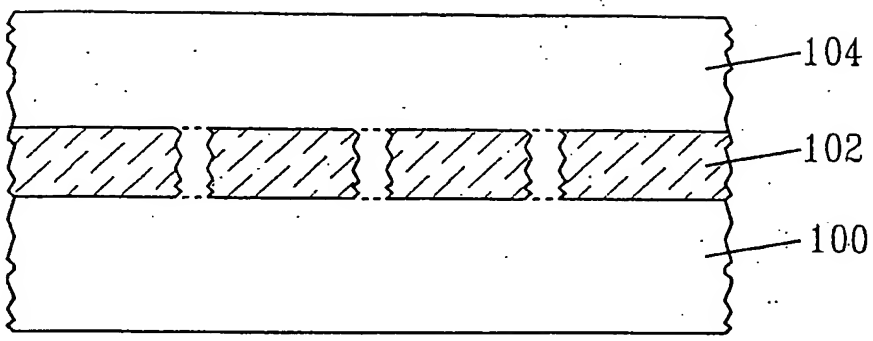

FIG. 1 (Prior Art)

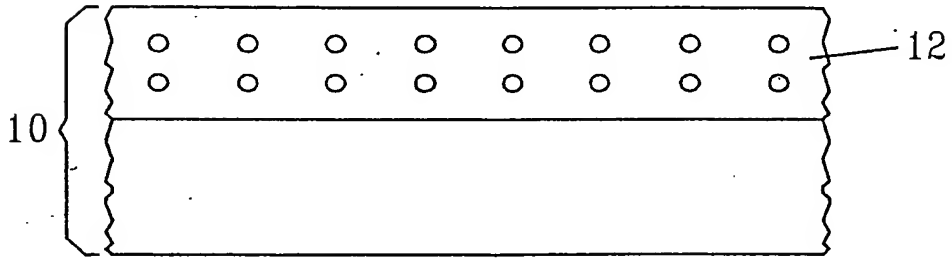

FIG. 2A

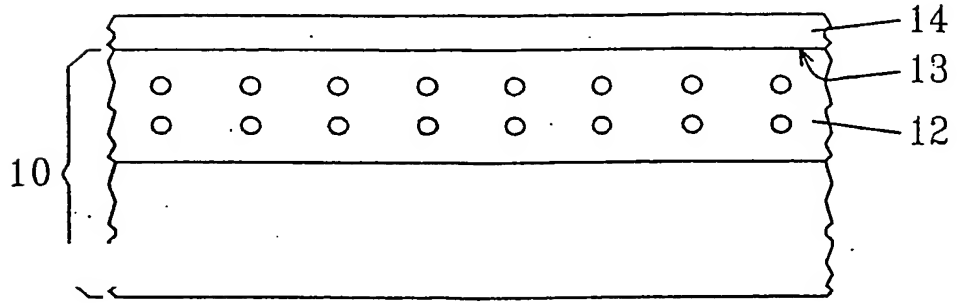

FIG. 2B

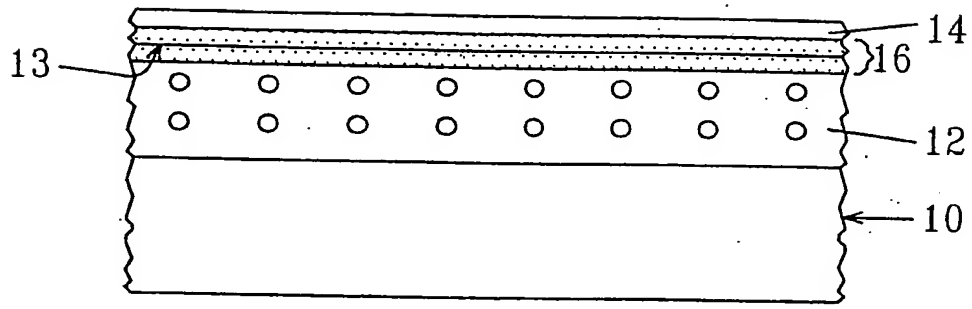

FIG.2C

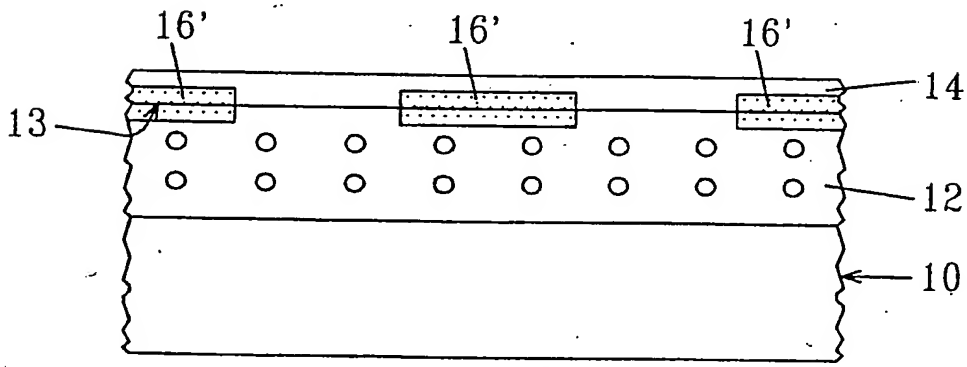

FIG.2D

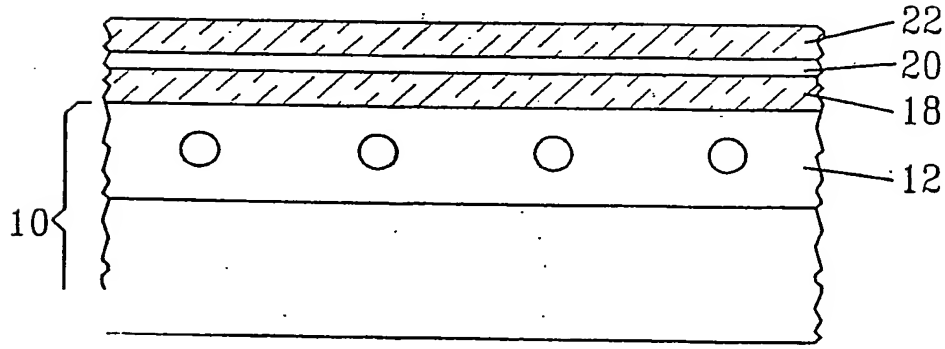

FIG.2E

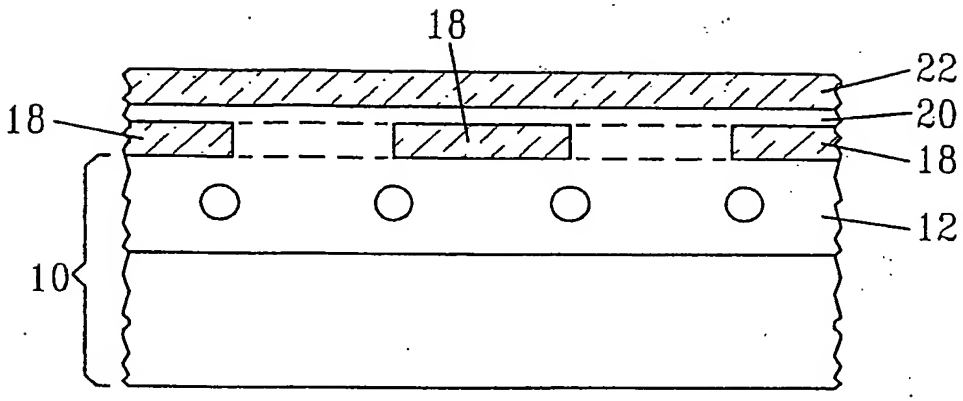

FIG.2F

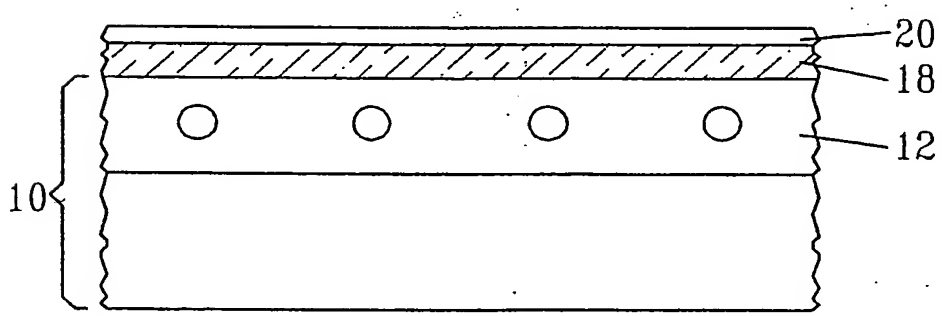

FIG.2G

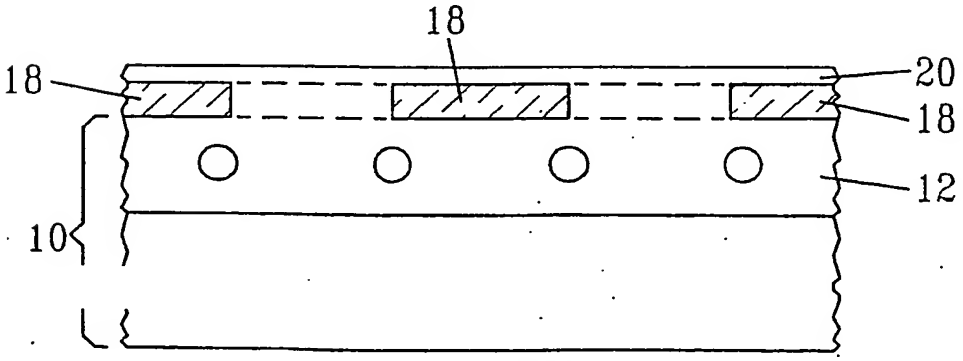

FIG.2H

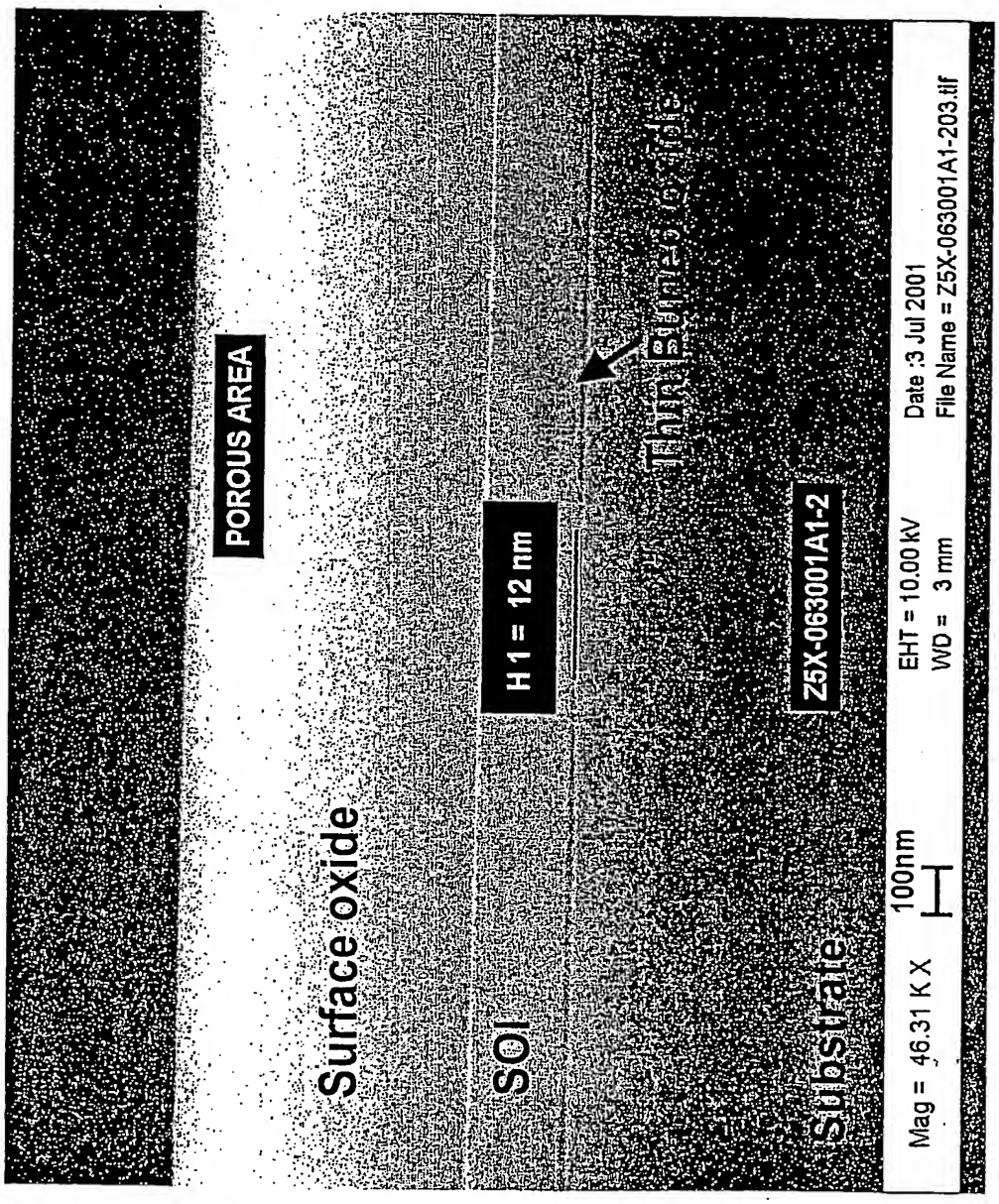
POROUS AREA
Surface oxide
SOI
H 1 = 12 nm
Substrate
Z5X-063001A1-2
Mag = 46.31 K X
100nm
EHT = 10.00 kV
WD = 3 mm
Date :3 Jul 2001
File Name = Z5X-063001A1-203.tif

Figure 3A

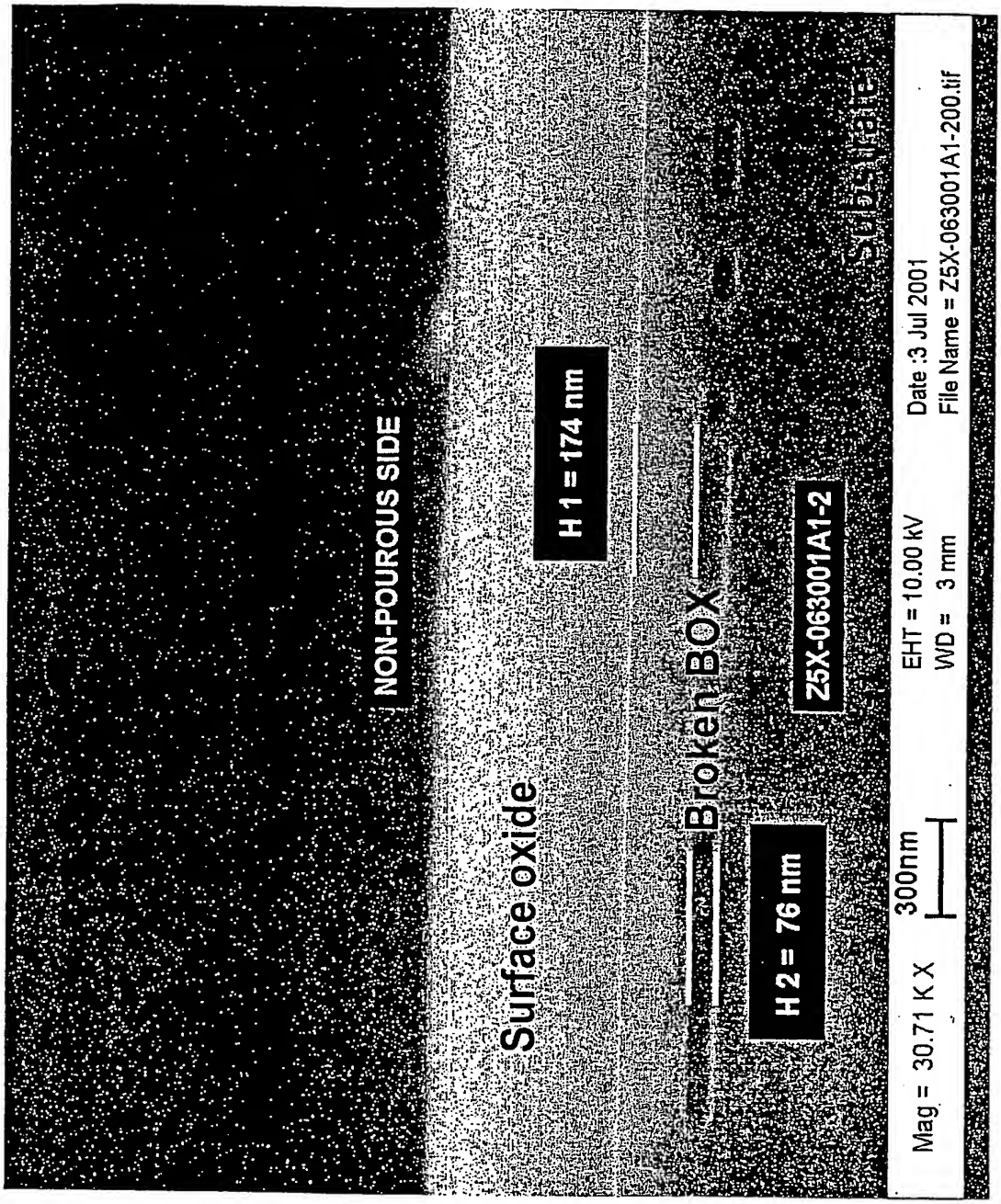
NON-POUROUS SIDE
Surface oxide
H 1 = 174 nm
Broken BOX
H 2 = 76 nm
Z5X-063001A1-2
Substrate
Mag = 30.71 K X
300nm
EHT = 10.00 kV
WD = 3 mm
Date :3 Jul 2001
File Name = Z5X-063001A1-200.tif

Figure 3B

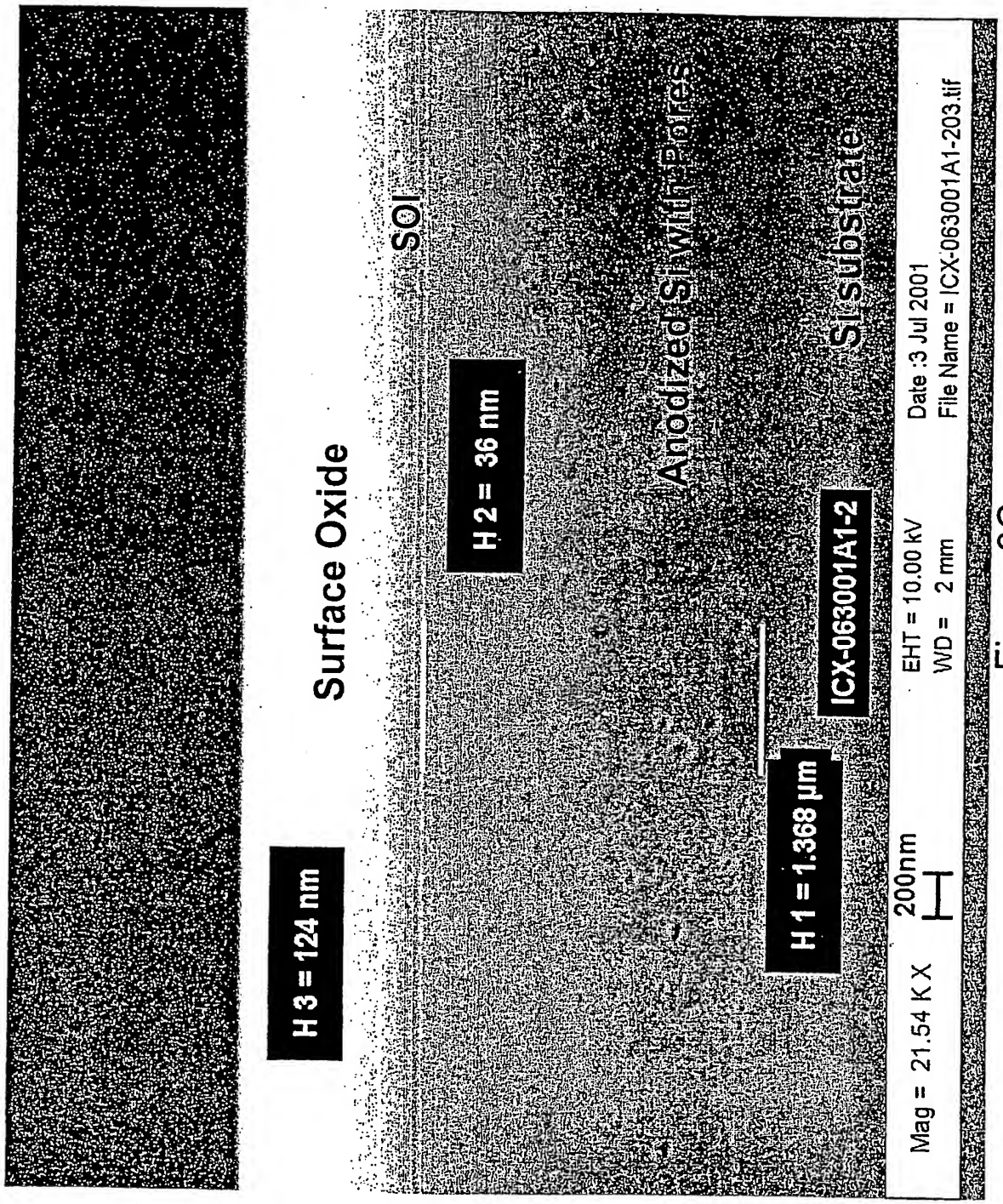
H 3 = 124 nm
Surface Oxide
SOI
H 2 = 36 nm
Anodized Si with pores
Si substrate
H 1 = 1.368 µm
ICX-063001A1-2
Mag = 21.54 K X
200nm
EHT = 10.00 kV
WD = 2 mm
Date :3 Jul 2001
File Name = ICX-063001A1-203.tif

Figure 3C

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